VDIC SYNCHRONOUS DYNAMIC RAM

VD2D4G72XX191XX3U6 USER MANUAL

Version : A4

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Contents

VDIC-DDR2 SDRAM

HIGH-SPEED 1.8V 64M x 72bit

SYNCHRONOUS DYNAMIC RAM

1. DESCRIPTION

The VD2D4G72XX191XX3U6 is a 4608M bits DDR2 SDRAM, organized as 64M×72 bit. The device has five die, each die includes 1Gbit. The device has a 72-bit interface and is selected with specific #CS, CK , #CK and CKE. The device is useful for a variety of high bandwidth, high performance memory system applications.

2. FEATURES

_Clock frequency up to 400MHz

_8 internal banks for concurrent operation

_4-bit prefetch architecture

_Programmable CAS Latency: 3, 4, 5, 6 and 7

_Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6

_Write Latency = Read Latency-1

_Programmable Burst Sequence: Sequential or Interleave

_Programmable Burst Length: 4 and 8

_Automatic and Controlled Precharge Command

_Power Down Mode

_Auto Refresh and Self Refresh

_Refresh Interval: 7.8 □s (8192 cycles/64 ms)

_ODT (On-Die Termination)

_Weak Strength Data-Output Driver Option

_Bidirectional differential Data Strobe (Single-ended data-strobe is an optional feature)

_On-Chip DLL aligns DQ and DQs transitions with CK transitions

_DQS# can be disabled for single-ended data strobe

_Read Data Strobe supported (x8 only)

_Differential clock inputs CK and CK#

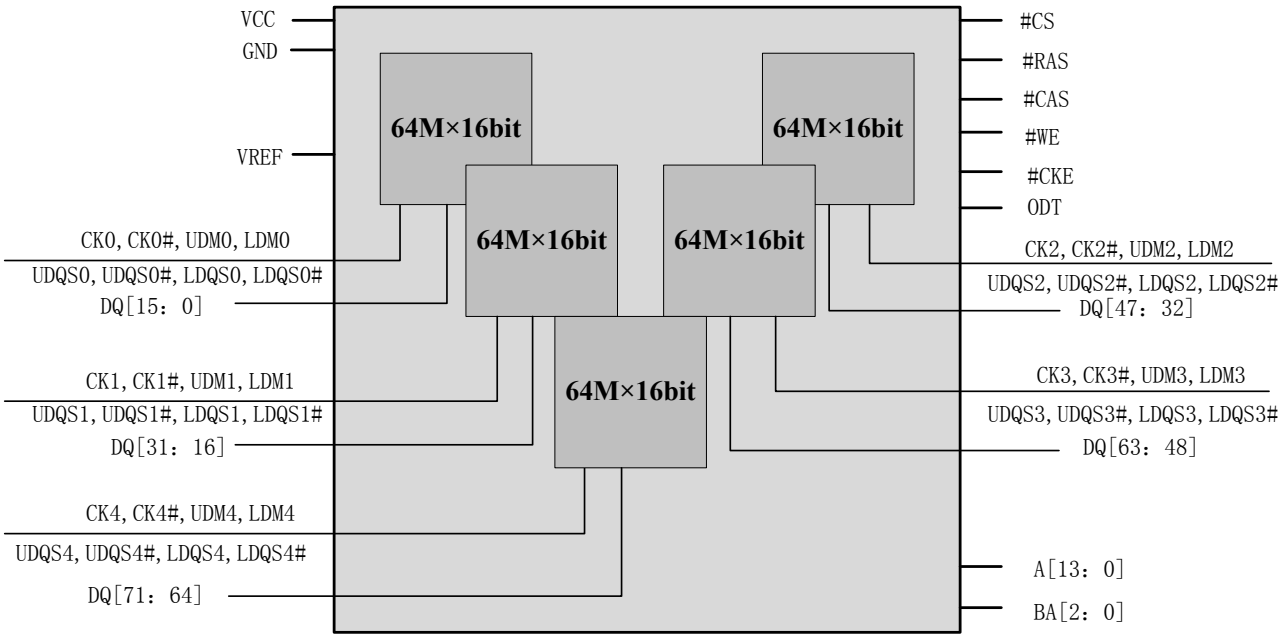
_VDD and VDDQ = 1.8V ± 0.1V

_PASR (Partial Array Self Refresh)

_SSTL_18 interface

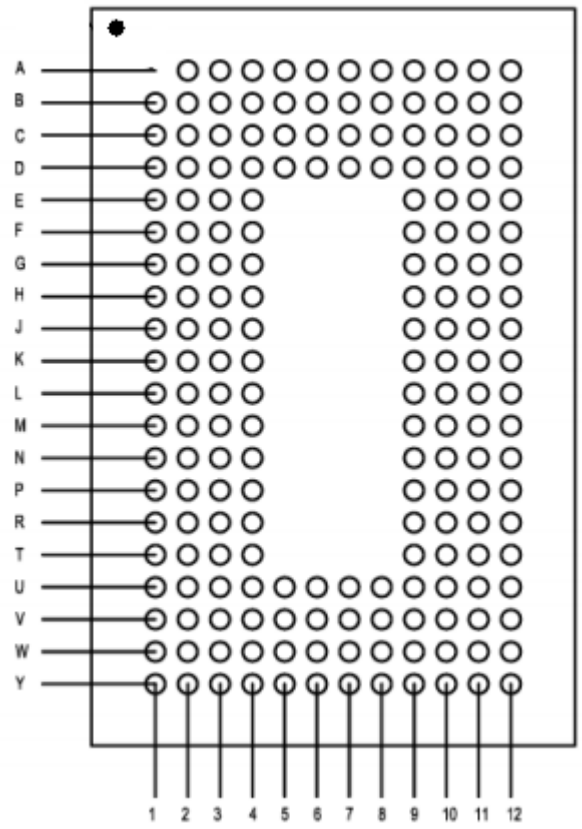
_tRAS lockout support

3. BLOCK DIAGRAM



4. PIN DESCRIPTIONS

Pin Id	Pin#		Pin Id	Pin Id	Pin#		Pin Id
	A1	E1	DQ60	NC	L1	U1	DQ26
CK3#	A2	E2	GND	A9	L2	U2	LDQS1
UDQS3#	A3	E3	DQ59	A10	L3	U3	DQ27
VCC	A4	E4	DQ54	GND	L4	U4	DQ20
NC	A5	E9	VCC	NC	L9	U5	LDQS4#
NC	A6	E10	UDQS2	GND	L10	U6	DQ67
VREF	A7	E11	UDQS2#	BA0	L11	U7	GND
DQ35	A8	E12	NC	WE#	L12	U8	UDM0
DQ44	A9	F1	NC	CK1#	M1	U9	DQ15
VCC	A10	F2	ODT	CK1	M2	U10	NC
LDM2	A11	F3	DQ62	UDQS4	M3	U11	LDM0
CK2#	A12	F4	DQ57	UDQS4#	M4	U12	DQ3
CK3	B1	F9	GND	CK4#	M9	V1	LDQS1#
DQ58	B2	F10	DQ47	NC	M10	V2	DQ16
UDQS3	B3	F11	DQ45	NC	M11	V3	DQ22
DQ61	B4	F12	DQ39	NC	M12	V4	DQ69
LDQS3#	B5	G1	NC	NC	N1	V5	LDQS4
DQ50	B6	G2	A8	NC	N2	V6	NC
GND	B7	G3	A4	DQ21	N3	V7	DQ70
DQ33	B8	G4	GND	DQ23	N4	V8	DQ0
DQ41	B9	G9	NC	CK4	N9	V9	LDQS0#
DQ46	B10	G10	DQ37	LDM4	N10	V10	UDQS0#
DQ34	B11	G11	GND	UDM4	N11	V11	UDQS0
CK2	B12	G12	A13/RFU	GND	N12	V12	CK0
NC	C1	H1	NC	VCC	P1	W1	DQ18
UDM3	C2	H2	A0	NC	P2	W2	DQ25
LDM3	C3	H3	VCC	DQ29	P3	W3	DQ19
NC	C4	H4	CS#	DQ31	P4	W4	DQ71
LDQS3	C5	H9	GND	NC	P9	W5	VREF
DQ48	C6	H10	CAS#	NC	P10	W6	DQ66
DQ53	C7	H11	CKE	DQ14	P11	W7	DQ68
DQ38	C8	H12	BA1	DQ9	P12	W8	DQ5
GND	C9	J1	NC	LDM1	R1	W9	LDQS0
UDM2	C10	J2	RAS#	UDM1	R2	W10	DQ13
LDQS2	C11	J3	A2	UDQS1#	R3	W11	GND
DQ32	C12	J4	A6	UDQS1	R4	W12	CK0#
DQ52	D1	J9	VCC	DQ1	R9	Y1	VCC
DQ51	D2	J10	A1	DQ12	R10	Y2	DQ28
DQ49	D3	J11	A5	DQ11	R11	Y3	DQ17
DQ63	D4	J12	VCC	DQ6	R12	Y4	GND
DQ56	D5	K1	NC	NC	T1	Y5	DQ64
DQ55	D6	K2	BA2	DQ24	T2	Y6	NC
DQ36	D7	K3	A11	GND	T3	Y7	DQ65
DQ43	D8	K4	GND	DQ30	T4	Y8	GND
DQ42	D9	K9	NC	NC	T9	Y9	DQ2
DQ40	D10	K10	A3	DQ10	T10	Y10	DQ7
LDQS2#	D11	K11	A12	DQ4	T11	Y11	VCC
VCC	D12	K12	A7	VCC	T12	Y12	DQ8



Symbol	Description
CK0~CK4, CK0#~CK4#	Input clocks
CKE	Clock enable
CS#	Chip Select
RAS#,CAS#,WE#	Command control inputs
A[13:0]	Address
BA[2:0]	Bank Address
DQ[71:0]	I/O
UDQS0~UDQS4, UDQS0#~UDQS4#	Upper Byte Data Strobe
LDQS0~LDQS4, LDQS0#~LDQS4#	Lower Byte Data Strobe
UDM0~UDM4	Upper Byte Input data mask
LDM0~LDM4	Lower Byte data mask
ODT	On Die Termination Enable
VCC	Supply voltage
GND	Ground
VREF	Reference voltage
NC	No connect

Note: VDDL and VSSDL are power and ground for the DLL.

5. DC OPERATING CONDITIONS

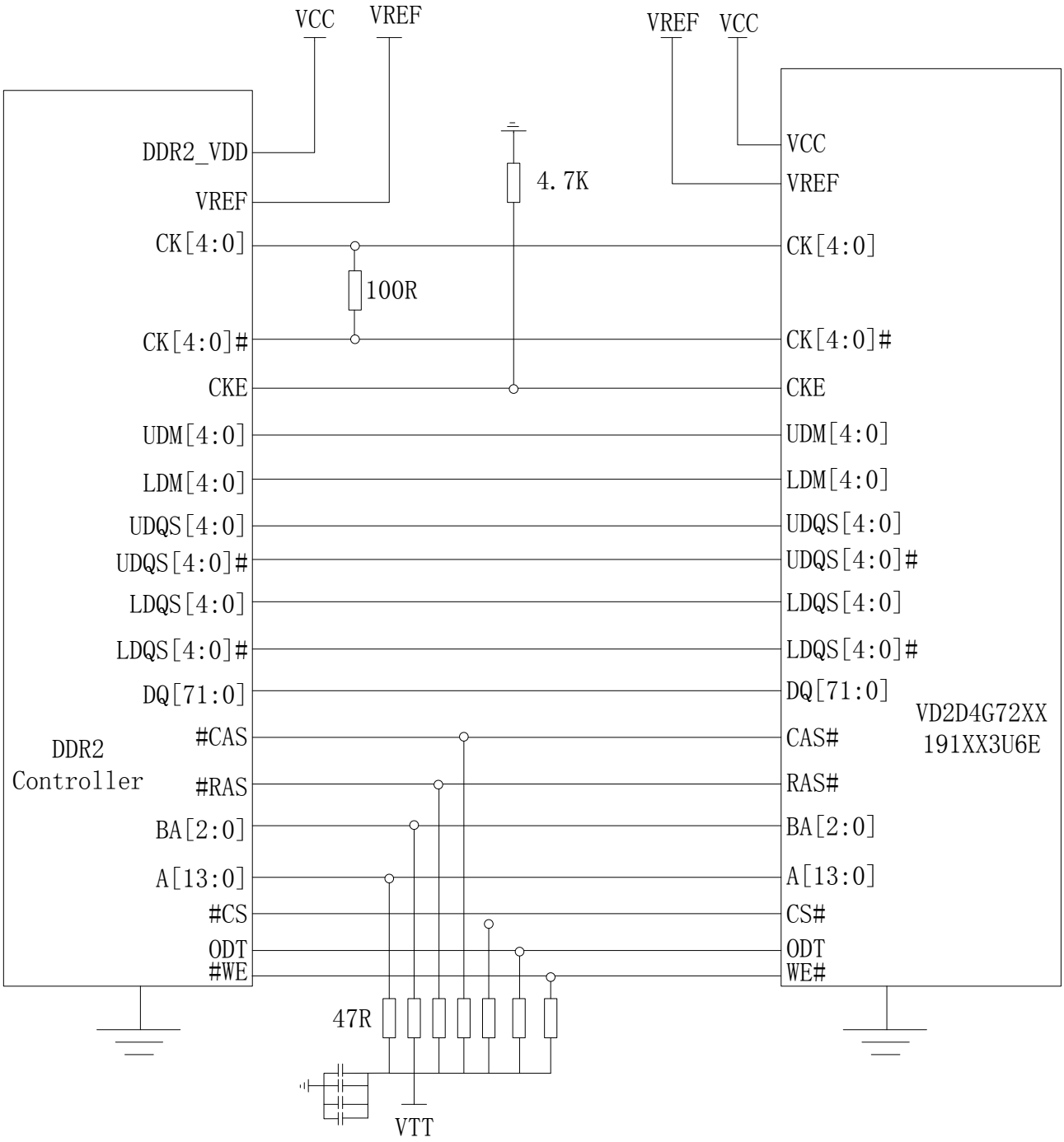
5.1. ABSOLUTE MAXIMUM DC RATINGS

Symbol	Parameter	Rating	Unit
VDD	Voltage on VDD pin relative to Vss	-1.0 to 2.3	V
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 to 2.3	V
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 to 2.3	V
Vin, Vout	Voltage on any pin relative to Vss	- 0.5 to 2.3	V
T_{OPR}	Operating Temperature Range	-40~ +105	℃
T_{STG}	Storage Temperature Range	-65 to +150	℃
I_I	Input Leakage Current	-5 to 5	uA
IOZ	Output Leakage Current	-5 to 5	uA
IVREF	VREF Leakage Current	-2 to 2	uA

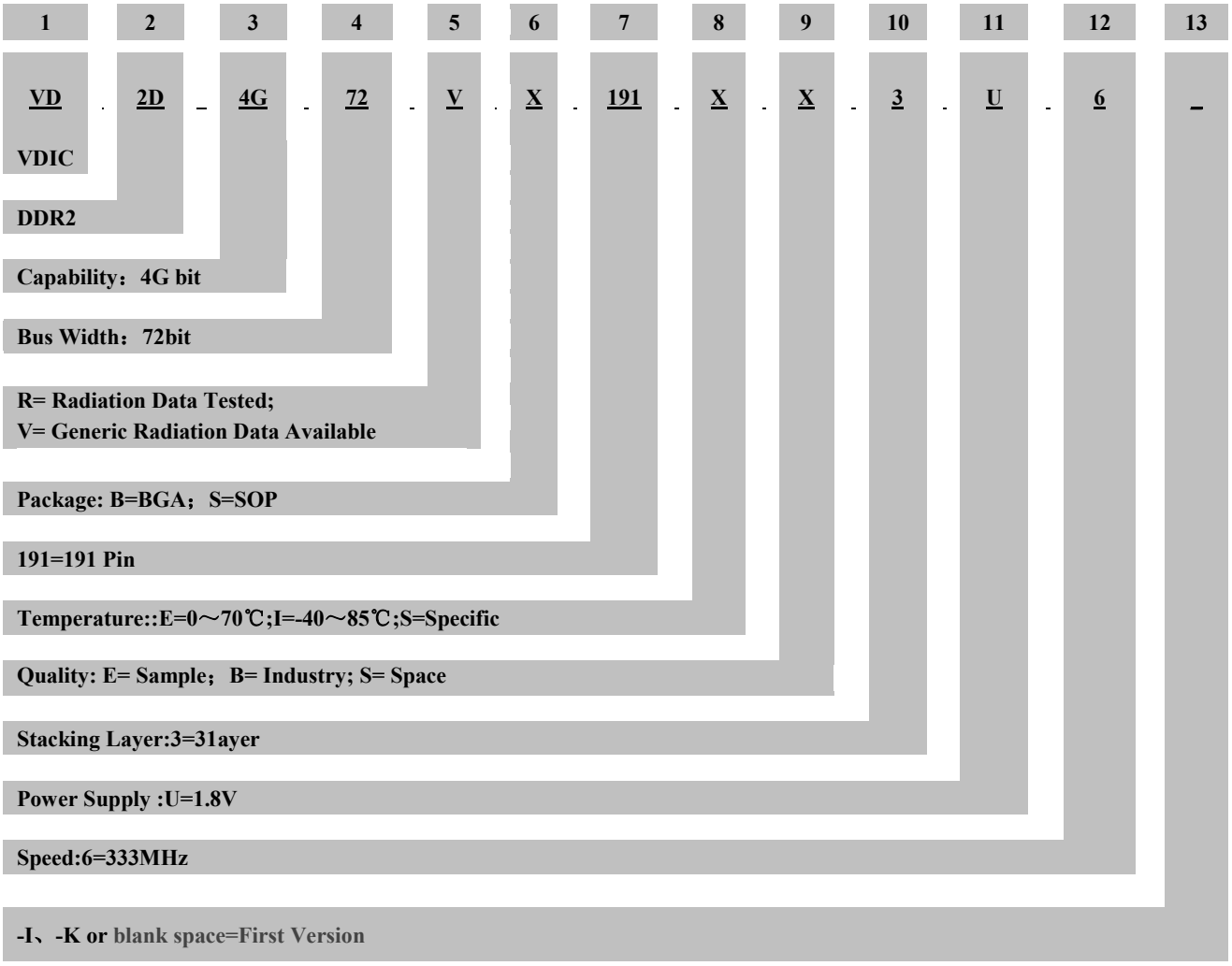
5.2. Recommended DC Operating Conditions (SSTL_1.8)

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	1.7	1.8	1.9	V
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	V
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V

6. TYPICAL APPLICATION



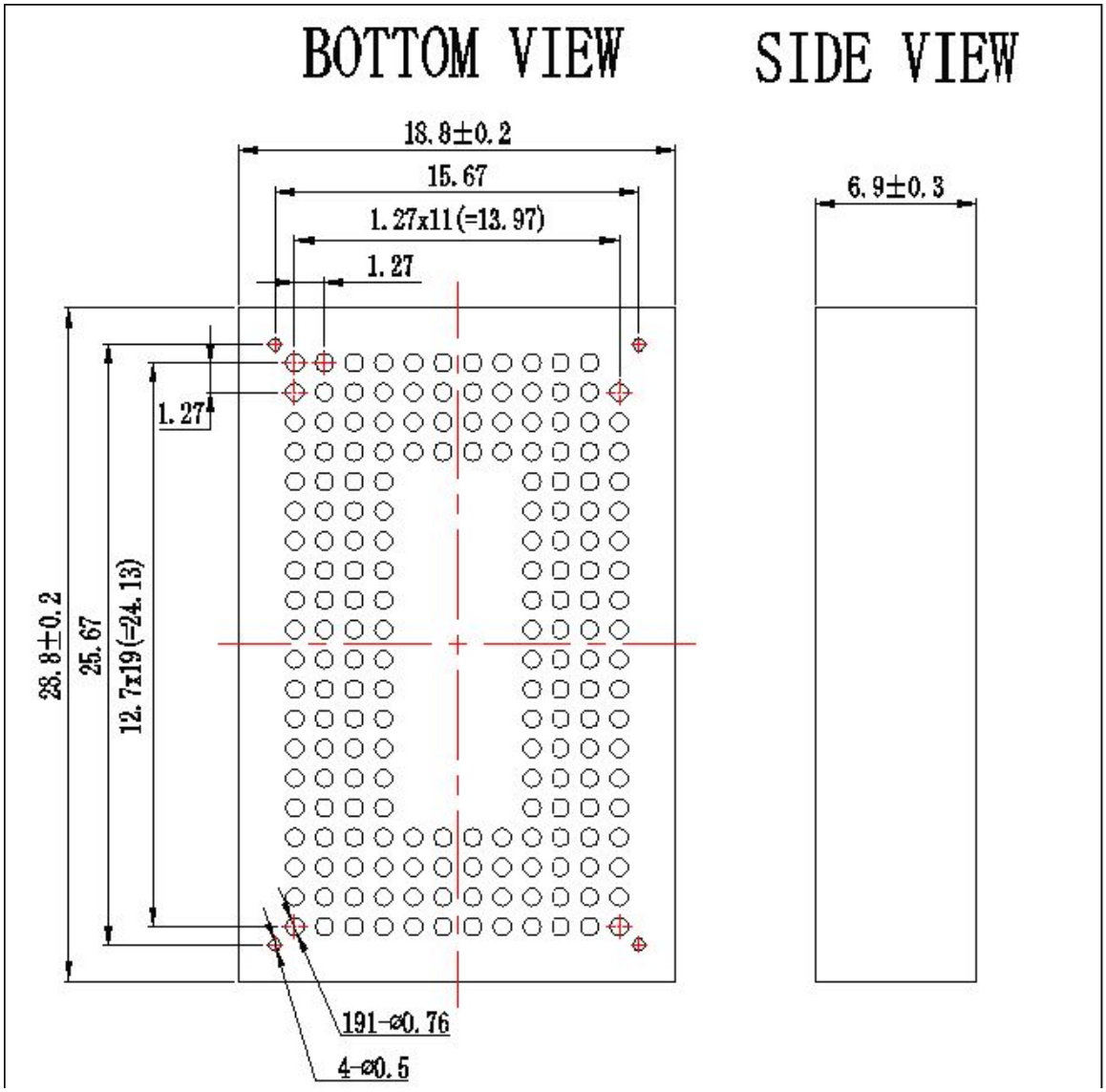
7. ORDERING INFORMATION



Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VD2D4G72VX191EE3U6	4G	72	-	-	-	-	0 ~ + 70
VD2D4G72VX191IB31U6	4G	72	-	-	-	-	-40 ~ + 85
VD2D4G72VX191IS31U6	4G	72	-	-	-	-	-40 ~ + 85
VD2D4G72RX191SS3U6	4G	72	100	>68	0.8	-	-40 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS



9. REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 5,2015	First Created
A1	Mar 15,2018	Add or reduce the chapters.
A2	Sep 27,2018	Correct pin descriptions
A3	Jay 30,2019	Modified ordering information
A4	Apr 19,2019	Modified typical application