VDIC DDR3 SYNCHRONOUS DYNAMIC RAM

VD3D16G16XB96XX2WH USER MANUAL

Version : B1

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VDIC-DDR3 SDRAM

HIGH-SPEED 1.35V/1.5V 1G x 16bit

SYNCHRONOUS DYNAMIC RAM

1. DESCRIPTION

The VD3D16G16XB96XX2WH is a 16Gbit DDR3 SDRAM high-density System-in-Package memory module.It is organized with 2 chips，each chip with a capacity of 8Gb(512Mx16).They can be addressed with separate CS#, CKE, ODT and ZQ.

The three-dimensional packaging technology is used to interconnect the multi-layer memory circuits to form a high-density DDR3 memory module with high reliability, high stability and miniaturization. It is particularly well suited for use in high reliability, high performance and high density system applications, such as servers or workstations.

2. FEATURES

- 96 balls JEDEC standard ball-out
- Combines two 512M×16bit devices in one package
- VDD=VDDQ = +1.35V(1.283V~1.45V)
- Backward compatible to VDD=VDDQ=1.5V±0.075V
- Clock frequency up to 667MHz
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- 8 internal banks per chip
- Nominal and dynamic on-die termination(ODT) for data,strobe,and mask signals
- Programmable CAS latency
- Programmable posted CAS additive latency
- Fixed burst lengths of 8 and burst chop (BC) of 4
- Selectable BC4 or BL8 on-the-fly
- Self refresh mode
- Write leveling
- Multipurpose register
- Output driver calibration
- Available temperature range :

  0℃~+70℃
  -40℃~+85℃
  -40℃~+105℃

3. BLOCK DIAGRAM

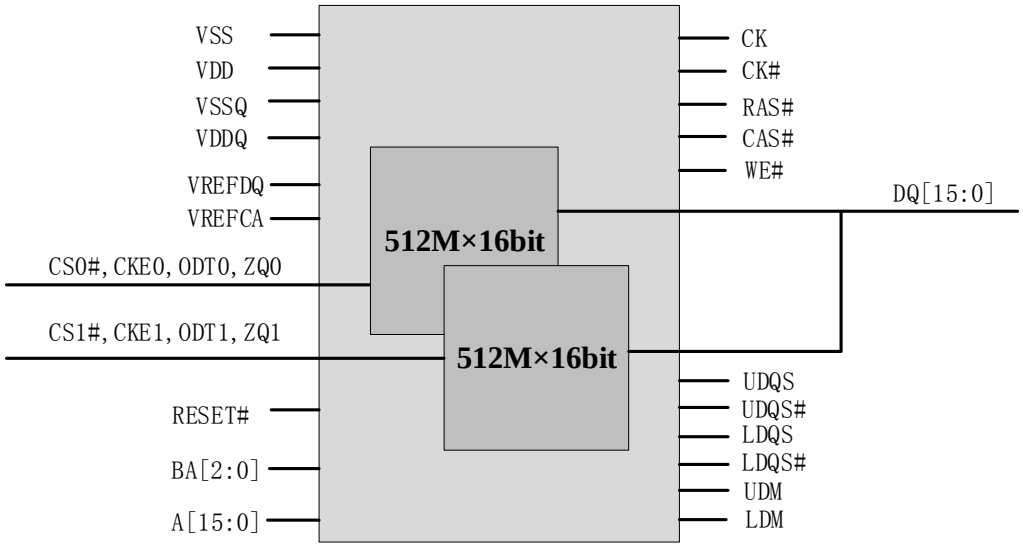

Figure 1 Block Diagram

4. PIN DESCRIPTIONS

Table 1 Pin list

Pin Id	Pin#			Pin Id	Pin Id	Pin#			Pin Id
VDDQ	A1		E1	VSS	ODT1	J1		N1	VDD
DQ13	A2		E2	VSSQ	VSS	J2		N2	A3
DQ15	A3		E3	DQ0	RAS#	J3		N3	A0
DQ12	A7		E7	LDM	CK	J7		N7	A12/BC#
VDDQ	A8		E8	VSSQ	VSS	J8		N8	BA1
VSS	A9		E9	VDDQ	CKE1	J9		N9	VDD
VSSQ	B1		F1	VDDQ	ODT0	K1		P1	VSS
VDD	B2		F2	DQ2	VDD	K2		P2	A5
VSS	B3		F3	LDQS	CAS#	K3		P3	A2
UDQS#	B7		F7	DQ1	CK#	K7		P7	A1
DQ14	B8		F8	DQ3	VDD	K8		P8	A4
VSSQ	B9		F9	VSSQ	CKE0	K9		P9	VSS
VDDQ	C1		G1	VSSQ	CS1#	L1		R1	VDD
DQ11	C2		G2	DQ6	CS0#	L2		R2	A7
DQ9	C3		G3	LDQS#	WE#	L3		R3	A9
UDQS	C7		G7	VDD	A10/AP	L7		R7	A11
DQ10	C8		G8	VSS	ZQ0	L8		R8	A6
VDDQ	C9		G9	VSSQ	ZQ1	L9		R9	VDD
VSSQ	D1		H1	VREFDQ	VSS	M1		T1	VSS
VDDQ	D2		H2	VDDQ	BA0	M2		T2	RESET#
UDM	D3		H3	DQ4	BA2	M3		T3	A13
DQ8	D7		H7	DQ7	A15	M7		T7	A14
VSSQ	D8		H8	DQ5	VREFCA	M8		T8	A8
VDD	D9		H9	VDDQ	VSS	M9		T9	VSS

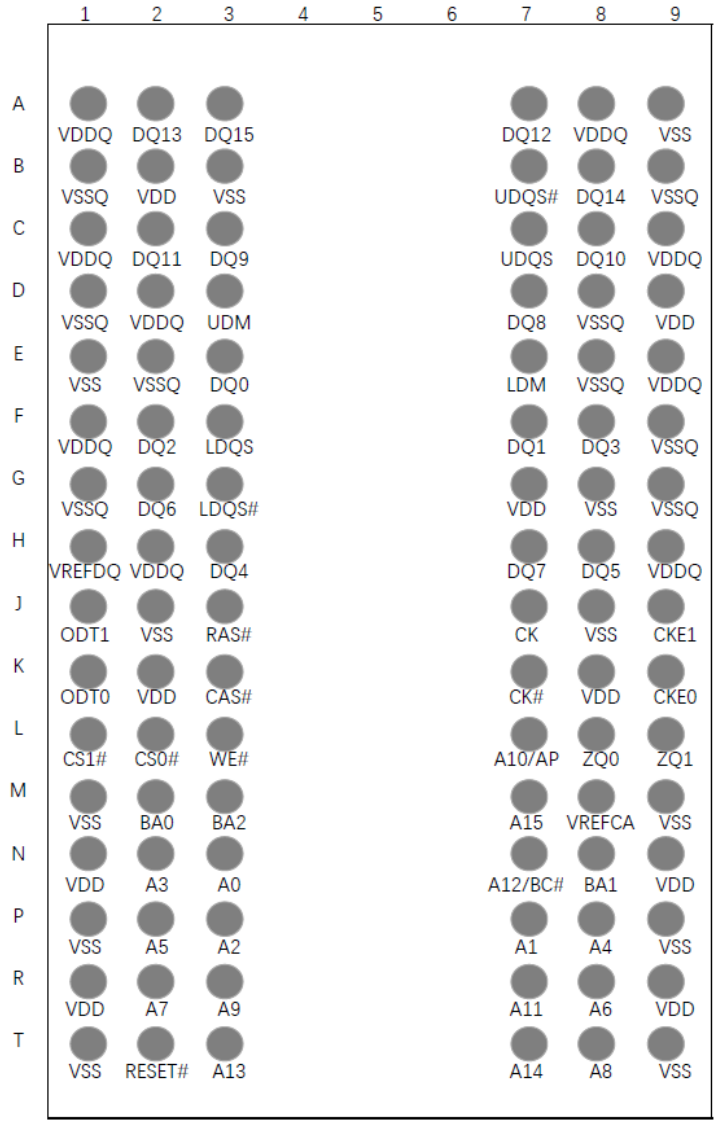

Figure 2 96-Ball BGA (Top View)

Table 2 Pin Descriptions

Symbol	Type	Description
CK,CK#	Input	Differential clock inputs.
CKE0,CKE1	Input	Clock enable.CKE enables(registered HIGH) and dissbles(registered LOW) internal circuitry and clocks on the DRAM.
CS0#,CS1#	Input	Chip Select.CS# enables(registered LOW) and disables (registered HIGHT) the command decoder.
ODT0,ODT1	Input	On Die Termination Enable. ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM.
RAS#,CAS#,WE#	Input	Command control inputs. RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.

Symbol	Type	Description
A[15:0]	Input	Address inputs.
A10/AP	Input	Autoprecharge.
A12/BC#	Input	Burst Chop.
BA[2:0]	Input	Bank Address inputs.
DQ[15:0]	I/O	Data input/output.Lower byte of bidirectional data bus(DQ[7:0]) ,Upper byte of bidirectional data bus(DQ[15:8]).
UDQS,UDQS#	I/O	Upper Byte Data Strobe.
LDQS,LDQS#	I/O	Lower Byte Data Strobe.
UDM	Input	Upper Byte Input data mask.
LDM	Input	Lower Byte data mask.
RESET#	Input	Active Low Asynchronous Reset. RESET# is an active LOW CMOS input referenced to VSS.
VDD	Supply	Power supply: 1.35V (1.283V-1.45V) / 1.5V ±0.075V (backward compatible).
VSS	Supply	Ground.
VDDQ	Supply	DQ power supply: 1.35V (1.283V-1.45V) / 1.5V ±0.075V (backward compatible).
VSSQ	Supply	DQ Ground.
VREFDQ	Supply	Reference Voltage for data.
VREFCA	Supply	Reference voltage for control, command, and address.
ZQ0,ZQ1	Reference	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	-	No connect.

5. DC OPERATING CONDITIONS

5.1. ABSOLUTE MAXIMUM DC RATINGS

Table 3 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Unit
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.975	V
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.975	V
Vin, Vout	Voltage on any pin relative to Vss	-0.4 ~ 1.975	V
T_c	Operating Temperature Range	-40 ~ +105	℃
T_{STG}	Storage Temperature Range	-55 ~ +150	℃

5.2. Recommended DC Operating Conditions

Table 4 Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	1.425	1.5	1.575	V
		1.283	1.35	1.45	
VDDQ	I/O Supply Voltage	1.425	1.5	1.575	V
		1.283	1.35	1.45	
VREFCA	Input reference voltage command/address bus	0.49×VDD	0.5×VDD	0.51×VDD	V
VREFDQ	I/O reference voltage DQ bus	0.49×VDD	0.5×VDD	0.51×VDD	V
VTT	Command/address termination voltage (system level, not direct DDR3 input)	-	0.5×VDDQ	-	V
VIH(DC90)	input logic high	VREF+0.09	—	VDD	V
VIH(DC100)		VREF+0.1	—	VDD	
VIL(DC90)	input logic low	VSS	—	VREF-0.09	V
VIL(DC100)		VSS	—	VREF-0.1	

6. Electrical Characteristics

Table 5 Electrical Characteristics

Parameter	Symbol	Value	Unit
Operating Current (one bank active)	I_{DD1}	177	mA
Precharge Power Down Current	I_{DD2P1}	86	mA
Room Temp Self Refresh	I_{DD6}	96	mA

7. TYPICAL APPLICATION

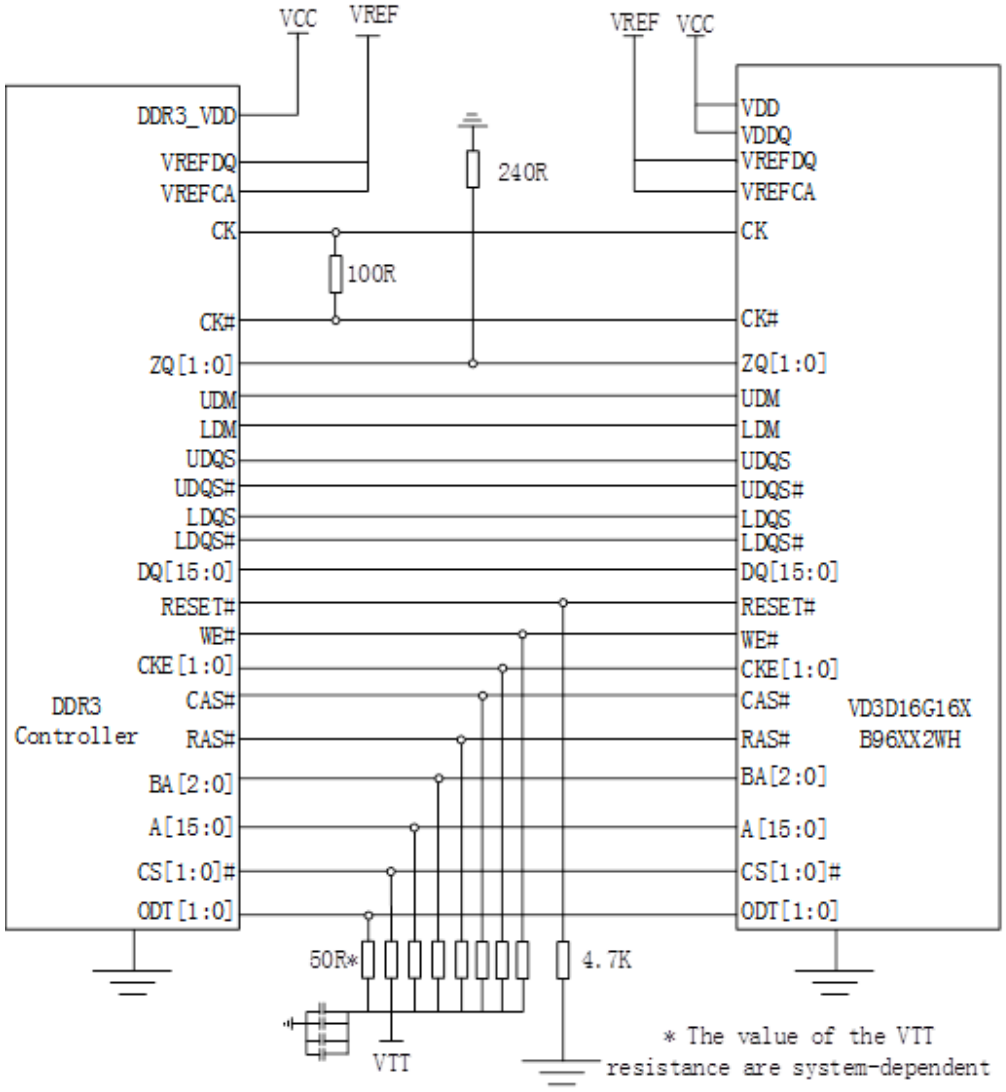

Figure 3 Typical Application

8. ORDERING INFORMATION

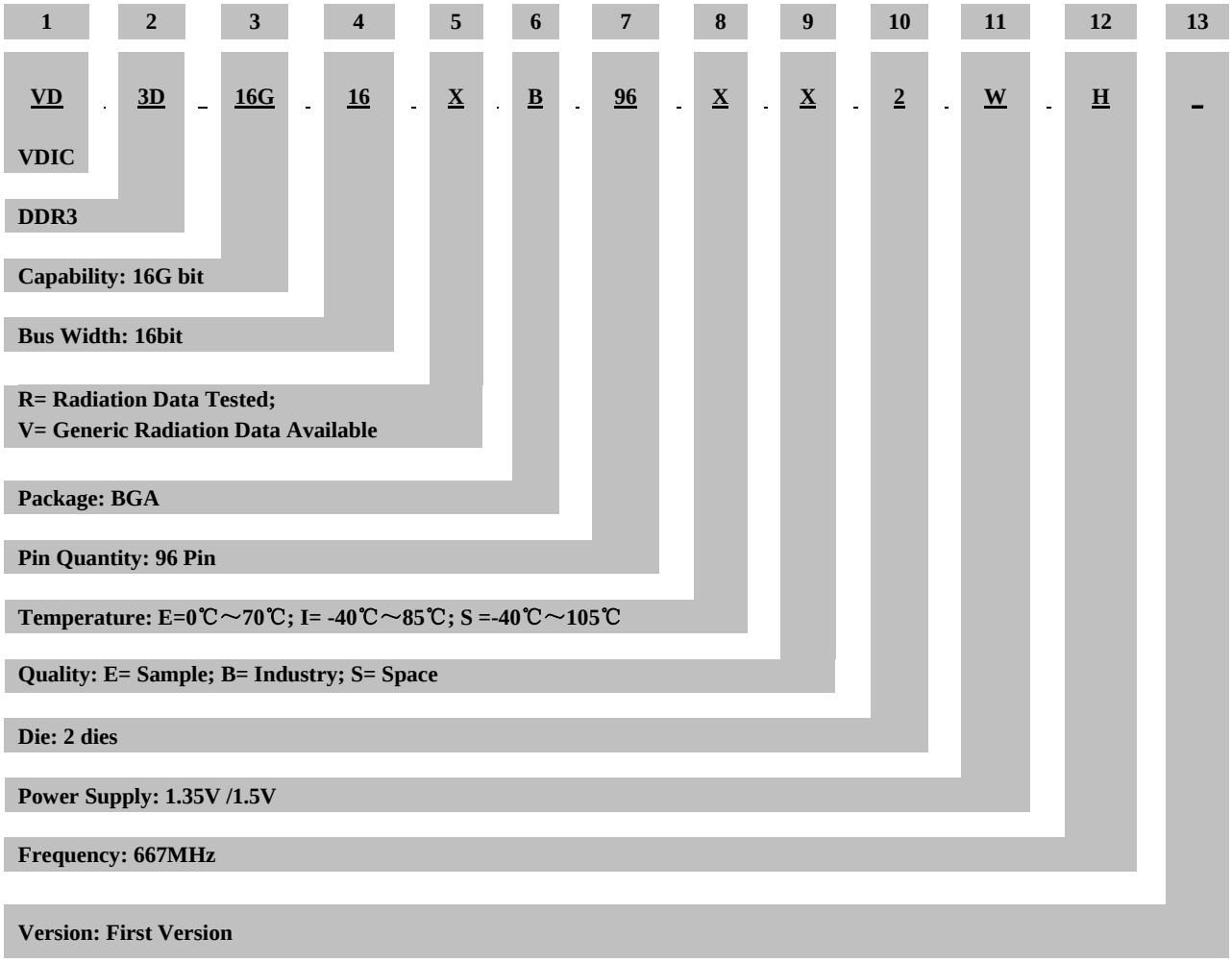

Table 6 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VD3D16G16VB96EE2WH	16G	16	-	-	-	BGA96	0~+70
VD3D16G16VB96IB2WH	16G	16	-	-	-	BGA96	-40~+85
VD3D16G16RB96SS2WH	16G	16	＞100	＞60	0.4	BGA96	-40~+105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm^2/mg）
[3] SEU:SEU Threshold （Mev.cm^2/mg）

PACKAGE DIMENSIONS

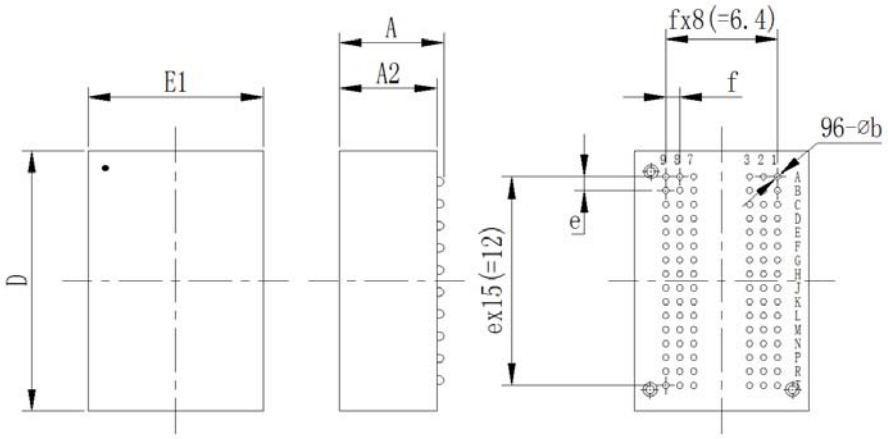

Figure 4 Package Dimensions

	最小值	最大值
A	5.6	6.2
A2	5.3	5.9
D	14.8	15.2
E1	10.2	10.4
b	0.35	
e	0.8	
f	0.8	
备注：1. 单位：mm		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Aug. 22,2018	First Created
A1	Jul. 8,2019	Change Package Dimensions
A2	Jul. 30,2019	Change Ordering Information
A3	Oct. 25,2019	Modify the description and some content.
B0	Mar 23,2020	Update TID and SEE
B1	Mar 09,2021	Update Package Dimension, TID and SEE