

# **VDIC NAND FLASH MEMORY**

## **VDNF64G16XS58XX8V25-II USER MANUAL**

**Version : A5**

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**Zhuhai Orbita Aerospace Science & Technology Co. , Ltd.**

**Add: Orbita Tech Park, NO.1 Baisha Road, Tangjia Dong ` an,**

**Zhuhai, Guangdong, China 519080**

**Tel: +86-756-3391979 Fax: +86-756-3391980**

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# VDIC-NAND Flash Memory

## HIGH-SPEED 3.3V 4G×16bit

### 1. DESCRIPTION

Offered in 4Gx16bit, the VDNF64G16XS58XX8V25-II is a 64G-bit NAND Flash Memory with spare capacity of 2048M-bits. The device operates at 3.3V. The I/O pins serve as the ports for address and data input/output as well as command input.

The VDNF64G16XS58XX8V25-II device is stacked with eight dies. A program operation can be performed in typical 200μs on the (4K+128)Byte page and an erase operation can be performed in typical 1.5ms on a (256K+8K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte.

Every die has an on-chip write controller which is used to automate all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the VDNF64G16XS58XX8V25-II 's extended reliability of 100K program/erase cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm.

Its NAND cell provides the most cost-effective solution for the solid state application market. The VDNF64G16XS58XX8V25-II is an optimum solution for large nonvolatile storage applications such as solid state data storage and advanced embedded control applications.

### 2. FEATURES

- Voltage Supply
  - 3.3V device: 2.7 ~ 3.6 V
- Organization
  - Memory Cell Array
    - 8dies x (1G + 32M)x 8 bit
  - Data Register for each die
    - (4K + 128) x 8bit
- Automatic Program and Erase
  - Page Program for each die
    - (4K + 128)Byte
  - Block Erase for each die
    - (256K + 8K)Byte
- Page Read Operation for each die
  - Page Size
    - (4K + 128)Byte
  - Random Access : 25μs(Max.)

- Serial Page Access : 25ns(Min.)
- Fast Write Cycle Time
  - Program time : 200μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : 100K Program/Erase Cycles
  - Data Retention : 10 Years
- Command Register Operation
- Intelligent Copy-Back with internal 1bit/528Byte EDC
- Package SOP-58

### 3. BLOCK DIAGRAM

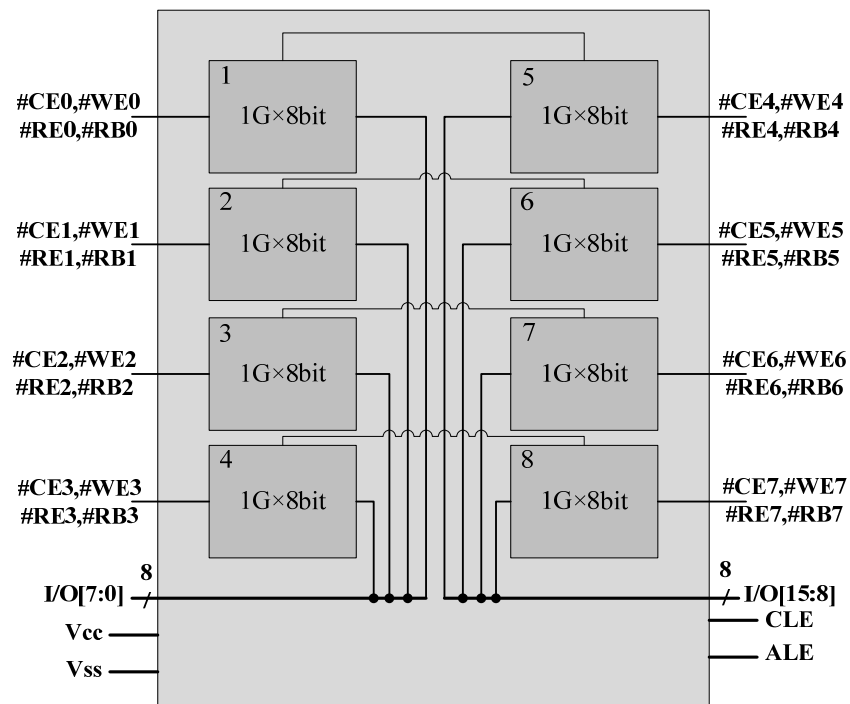


Figure 1 Block diagram

## 4. PIN DESCRIPTIONS -SOP-58

Pin Id	Pin #		Pin Id
#RE1	1	58	#RE6
#RE7	2	57	#RE5
#RB7	3	56	#RE4
#RB6	4	55	#RE3
#RB5	5	54	#RE2
#RB4	6	53	I/O14
#RB3	7	52	I/O15
#RB2	8	51	I/O7
#RB1	9	50	I/O6
#RB0	10	49	I/O5
#RE0	11	48	I/O4
#CE0	12	47	I/O12
#CE1	13	46	I/O13
#CE2	14	45	NC
VCC	15	44	VCC
VSS	16	43	VSS
#CE7	17	42	NC
NC	18	41	I/O10
CLE	19	40	I/O11
ALE	20	39	I/O3
#WE0	21	38	I/O2
#WP	22	37	I/O1
#WE7	23	36	I/O0
#WE1	24	35	I/O8
#WE2	25	34	I/O9
#WE3	26	33	#CE3
#WE4	27	32	#CE4
#WE5	28	31	#CE5
#WE6	29	30	#CE6

Figure 2 Pin configuration

Table 1: Pin description

Name	Function
I/O0~I/O15	<b>DATA INPUTS/OUTPUTS</b> The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	<b>COMMAND LATCH ENABLE</b> The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the #WE signal.
#CE0 (Die1)	<b>Die Enable Input</b> .When #CEn is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
#CE1 (Die2)	
#CE2 (Die3)	
#CE3 (Die4)	
#CE4 (Die5)	
#CE5 (Die6)	
#CE6 (Die7)	
#CE7 (Die8)	

Name	Function
ALE	<b>ADDRESS LATCH ENABLE</b> The ALE input controls the activating path for the address to the internal address registers. Addresses are latched on the rising edge of #WE with ALE high.
#REn	<b>READ ENABLE</b> The #REn input is the serial data-out control, and when active , drives the data onto the I/O bus. Data is valid $t_{REA}$ after the falling edge of #RE which also increments the internal column address counter by one.
#WEn	<b>WRITE ENABLE</b> The #WEn input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the #WE pulse.
#WP	<b>WRITE PROTECT</b> The #WP pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the #WP pin is active low.
#R/B0 (Die1)	<b>READY/BUSY OUTPUT</b> The #R/Bn output indicates the status of the device operation. When low it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
#R/B1 (Die2)	
#R/B2 (Die3)	
#R/B3 (Die4)	
#R/B4 (Die5)	
#R/B5 (Die6)	
#R/B6 (Die7)	
#R/B7 (Die8)	
VCC	<b>POWER</b> VCC is the power supply for device.
VSS	<b>GROUND</b>

**Notes :**

1. Connect all Vcc and Vss pins of each device to common power supply outputs.
2. Do not leave Vcc or Vss disconnected.

## 5. ELECTRICAL SPECIFICATIONS

### 5.1 Absolute Maximum Ratings

Table 2:Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on VCC supply relative to Vss	V <sub>CC</sub>	-0.6 ~ +4.6	V
Voltage on any pin relative to Vss	V <sub>IN</sub>	-0.6 ~ +4.6	V
Power Dissipation	P <sub>D</sub>	1.5	W
Operating Temperature Range	T <sub>OPR</sub>	-55 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

### 5.2 Recommended DC Operating Conditions

Table 3:Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	2.7	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	V <sub>CC</sub> ×0.8	—	V <sub>CC</sub> +0.3	V
Input low voltage	V <sub>IL</sub>	-0.3	—	V <sub>CC</sub> ×0.2	V

### 5.3 DC And Operating Characteristics

Table 4:DC And Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V <sub>OL</sub>	V <sub>CC</sub> =2.7V I <sub>OL</sub> =2.1mA	—	0.4	V
Output voltage high level	V <sub>OH</sub>	V <sub>CC</sub> =2.7V, I <sub>OH</sub> = -0.4mA	2.4	—	V

## 6. Typical Application

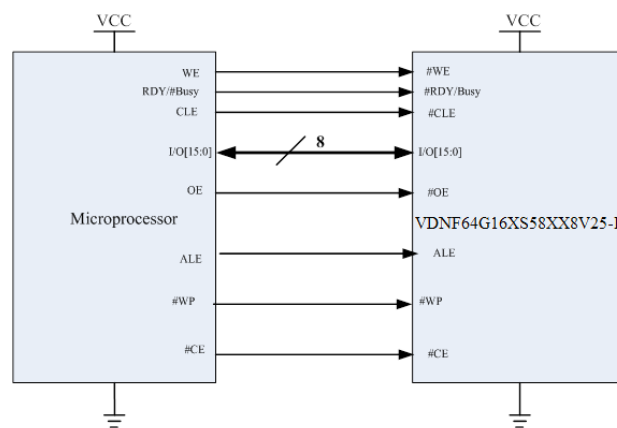


Figure 3 Typical application

## 7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>NF</u>	<u>64G</u>	<u>16</u>	<u>X</u>	<u>S</u>	<u>58</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>V</u>	<u>25</u>	<u>-II</u>
VDIC												
NAND FLASH												
Capability: 64G bit												
Bus Width: 16 bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 58 Pin												
Temperature: E=0~+70℃;I=-40~+85℃;M=-55~+125℃												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer: 8ayer												
Power Supply : 3.3V												
Speed: 25ns												
Version: Second Version												

Table 5:Part Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID <sup>1</sup>	SEL <sup>2</sup>	SEU <sup>3</sup>		
VDNF64G16VS58EE8V25-II	64G	16	-	-	-	SOP58	0 ~ +70
VDNF64G16VS58IB8V25-II	64G	16	-	-	-	SOP58	-40 ~ +85
VDNF64G16VS58MM8V25-II	64G	16	-	-	-	SOP58	-55 ~ +125
VDNF64G16RS58MS8V25-II	64G	16	>60	>60	1.3	SOP58	-55 ~ +125

<sup>1</sup> TID: Total Dose (Krad(Si))

<sup>2</sup> SEL: LET Threshold (Mev.cm<sup>2</sup>/mg)

<sup>3</sup> SEU:SEU Threshold (Mev.cm<sup>2</sup>/mg)



### 8. PACKAGE DIMENSIONS

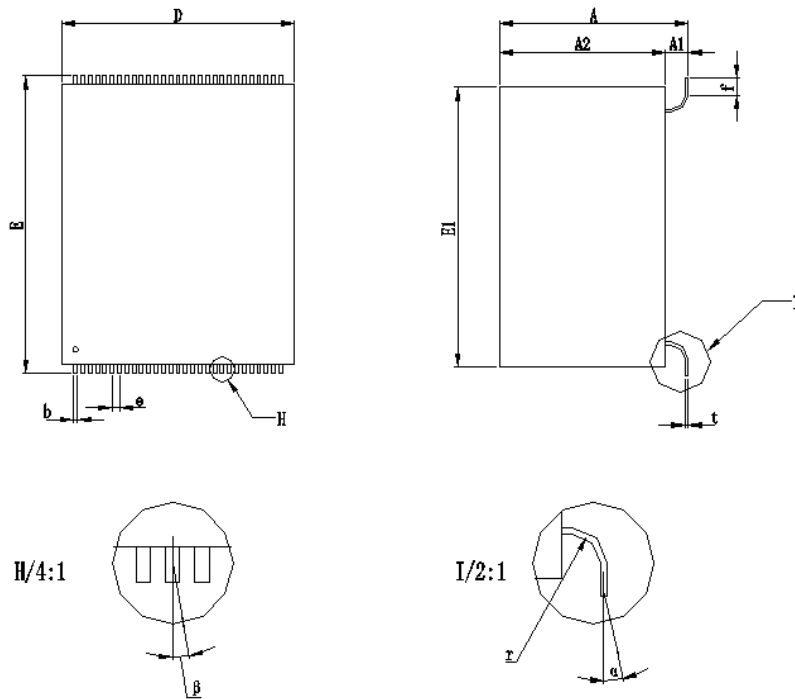


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	15.60	16.00
E	19.80	20.20
E1	18.80	19.20
f	1.20	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
$\alpha$	$\leq 3^\circ$	
$\beta$	$\leq 3^\circ$	
NOTE: 1. Unit: mm 2. $A1 = A - A2$		

## 9. REVISION HISTORY

**Table 7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Description of Change</b>
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Apr 25,2018	Add or reduce chapters