VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY

VDMR64M08XS54XX4V35 USER MANUAL

Version : B1

Contents

VDIC-MRAM

HIGH-SPEED   3.3V   8M × 8bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1. DESCRIPTION

The VDMR64M08XS54XX4V35 is a 4×16,777,216-bit high-speed access time, high-density Magnetoresistives Random Access Memory device. Manufactured with VDIC Very Dense SiP technology, this Die stacks four 16-Mbit MRAM Dies. It is organized as four independent dies of 2Mx 8bit wide data interface.

The VDMR64M08XS54XX4V35 offers MRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR64M08XS54XX4V35 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.
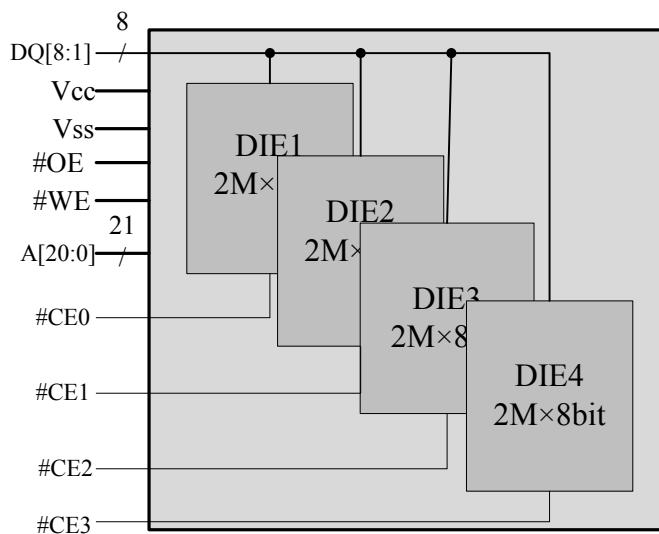
The VDMR64M08XS54XX4V35 has four dies. Each die can be selected separately with dedicated #CEn. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDMR64M08XS54XX4V35 is available in a 54-pin SOP package.

2. FEATURES

- Fast 35ns Read/Write Cycle

- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign

- Unlimited Read & Write Endurance

- Data Always Non-volatile for >20-years at storage temperature

- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design

- Stack of four 16Mbit MRAM

- Organized as 4 dies of 2M x 8 bit memory

- Four independent Die Select

- 3.3 Volt Power Supply

- Automatic Data Protection on Power Loss

- 54-lead SOP   package

3. BLOCK DIAGRAM

(All other signals are common to the four memories)
Figure 1 Block diagram

4. PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
NC	1	54	NC
#CE3	2	53	NC
DC	3	52	DC
A20	4	51	A19
A0	5	50	DC
A1	6	49	A18
A2	7	48	A17
A3	8	47	A16
A4	9	46	A15
#CE0	10	45	#OE
DQ1	11	44	DQ8
DQ2	12	43	DQ7
VDD	13	42	VSS
VSS	14	41	VDD
DQ3	15	40	DQ6
DQ4	16	39	DQ5
#WE	17	38	DC
A5	18	37	A14
A6	19	36	A13
A7	20	35	A12
A8	21	34	A11
A9	22	33	A10
DC	23	32	DC
DC	24	31	DC
#CE1	25	30	NC
#CE2	26	29	NC
NC	27	28	NC
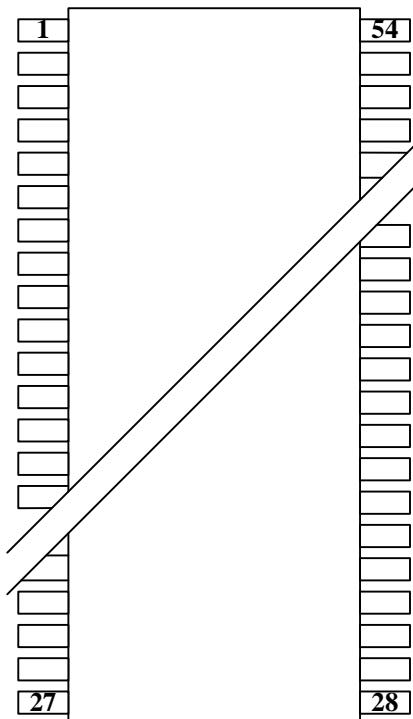
Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CE0	Die select	Disables or enables memory die 1 operation
#CE1	Die select	Disables or enables memory die 2 operation
#CE2	Die select	Disables or enables memory die 3 operation
#CE3	Die select	Disables or enables memory die 4 operation
A0 ~ A20	Address	20-bit addresses
#WE	Write enable	Enables write operation common to all memory dies
#OE	Output enable	Enables data output common to all memory dies
DQ1~ DQ8	Data input/output	Data inputs/outputs 8-bit wide bus
VDD/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	These pins are recommended to be left No Connection on the device.
DC	Do not connect	These pins do not connect

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than the maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on VDD supply relative to Vss	VDD	-0.5 ~ +4.0	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ VDD +0.5	V
Power Dissipation	P_D	**< 1.0**	W
Operating Temperature Range	T_{OPR}	-55 ~ +95	℃
Storage Temperature Range	T_{STG}	-55 ~ +105	℃

5.2. RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.2	——	V_{DD}+0.3	V
Input low voltage	V_{IL}	-0.5	——	0.8	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 4 DC electrical characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	I_{OL}= +4mA	—	0.4	V
Output voltage high level	V_{OH}	I_{OL}= -4mA	2.4	—	V

6. TYPICAL APPLICATION
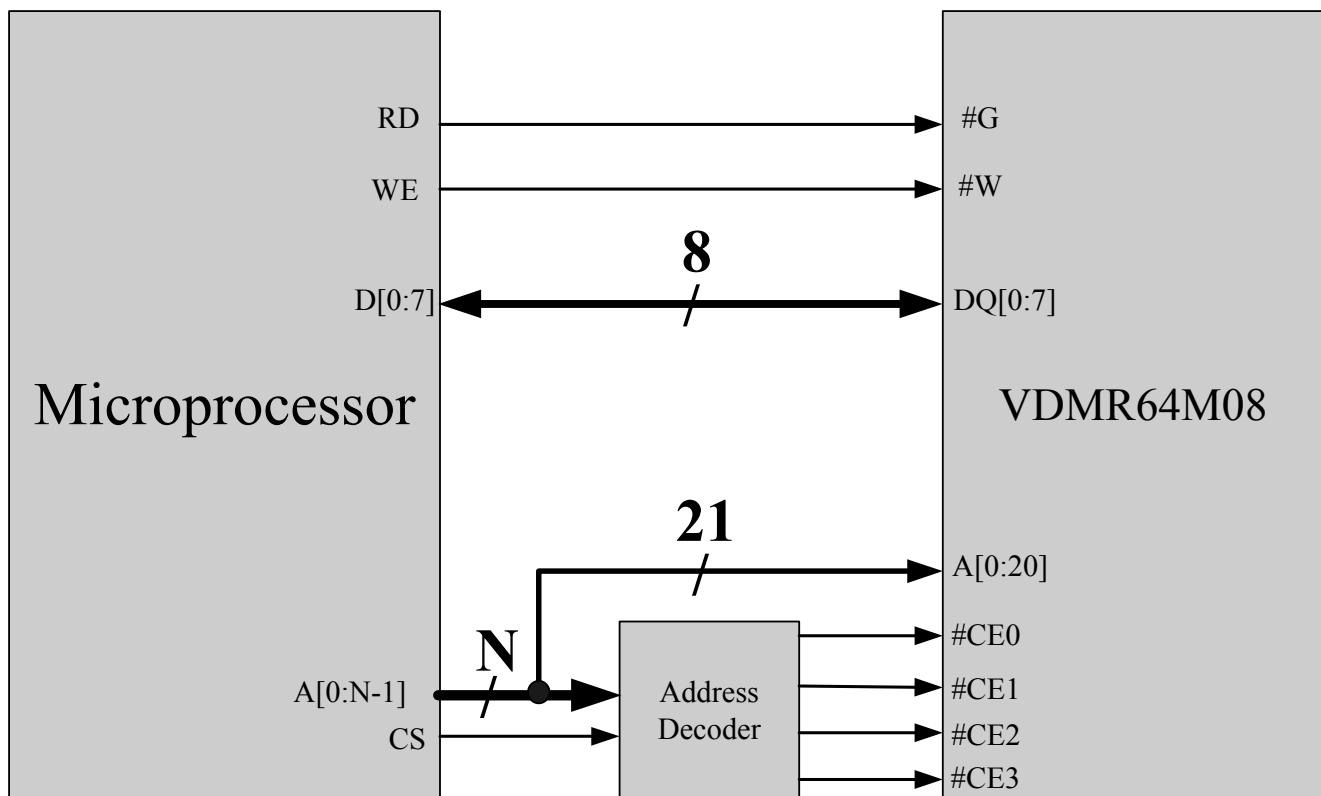
Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13

VD - **MR** - **64M** - **08** - **X** . **S** - **54** - **X** - **X** - **4** . **V** - **35** _

VDIC

MRAM

Capability: 64M bit

Bus Width: 8bit

R= Radiation Data Tested;
V= Generic Radiation Data Available

Package: SOP

Pin Quantity: 54 Pin

Temperature: E=0～＋70℃; I=-40～＋85℃; S=-55～＋95℃

Quality: E= Sample; B= Industry; S= Space

Stacking Layer: 4 layer

Power Supply: 3.3V

Speed: 35ns

Version: First Version

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature （℃）
			TID[1]	SEL[2]	SEU[3]		
VDMR64M08VS54EE4V35	64M	8	-	-	-	SOP54	0 ～ ＋70
VDMR64M08VS54IB4V35	64M	8	-	-	-	SOP54	-40 ～ ＋85
VDMR64M08RS54SS4V35	64M	8	> 50	> 75	> 15	SOP54	-55 ～ ＋95

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[1] TID: Total Dose （Krads(Si)）

[2] SEL: LET Threshold （Mev.cm2/mg）

[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS
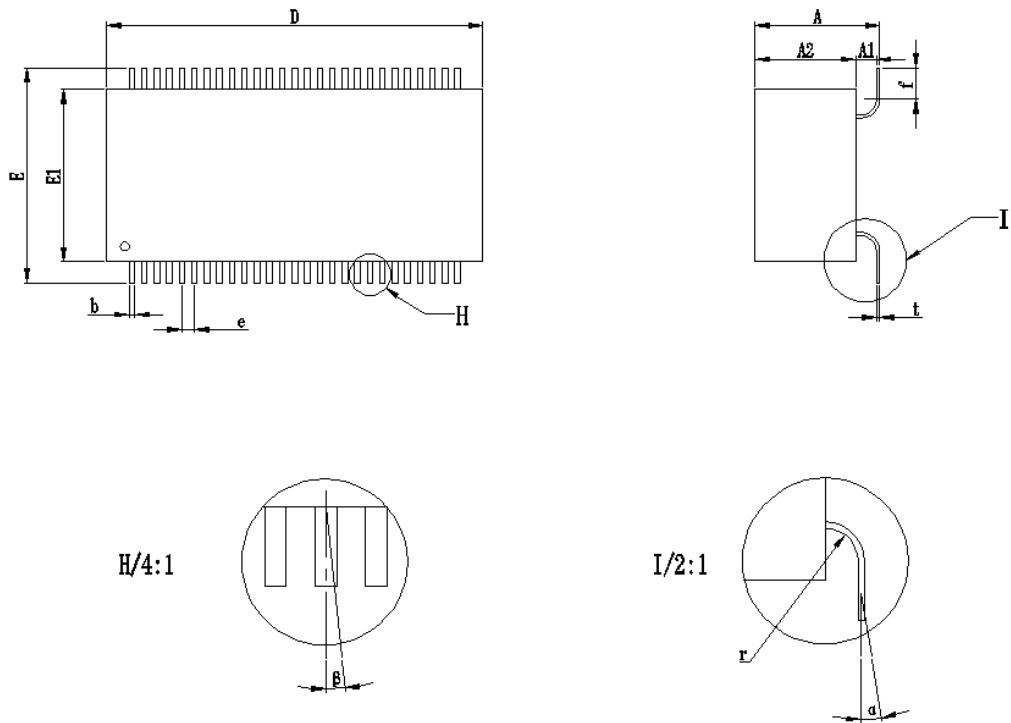
Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Mar 9,2018	Add or reduce chapters
B0	May 22, 2018	Modified Operating Temperature Range and Storage temperature.
B1	Mar 21,2020	Update TID and SEE