VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD4G08XS54XX8V75 USER MANUAL

Version : B0

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VDIC-SDRAM

HIGH-SPEED 3.3V 512M×8Bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

The VDSD4G08XS54XX8V75 is a 4,096M bits SDRAM, organized as 512M words×8bits. The device has 8 dies, each die includes 33,554,432 words×8bits×4bank, and a chip select. All inputs and outputs are referred to the rising edge of the clock. The device is useful for a variety of high bandwidth, high performance memory system applications. It is packaged in standard 54-pin TSOP.

2 FEATURES

- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Single pulsed #RAS
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8, full page
- 2 variations of burst sequence
  - Sequential (BL=1, 2, 4, 8, full page)
  - Interleave (BL=1, 2, 4, 8)
- Programmable #CAS latency (CL): 2, 3
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
  - Auto refresh
  - Self refresh

3 BLOCK DIAGRAM

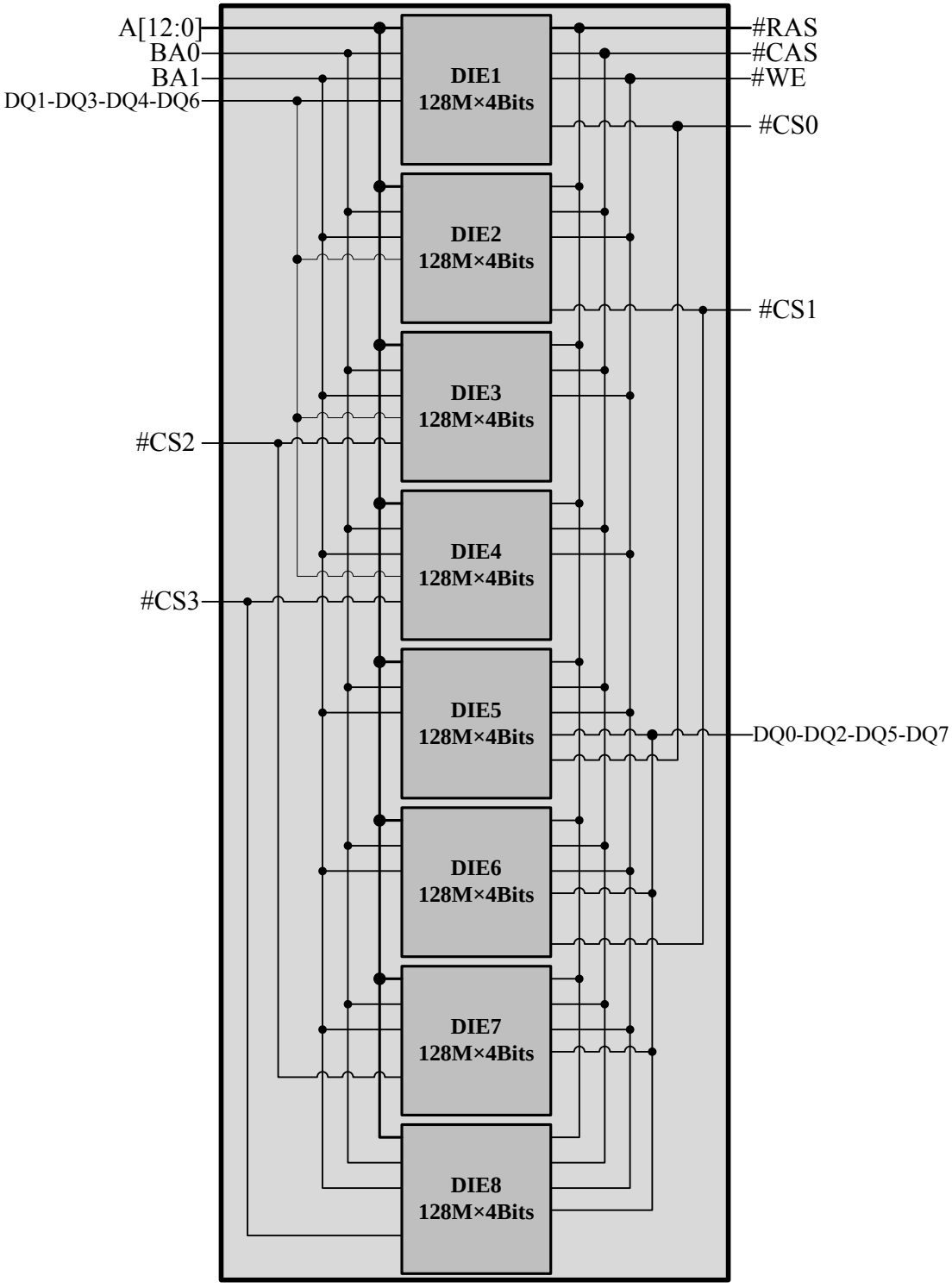

Figure 1: Signal link of Block Diagram

4 PIN DESCRIPTIONS

Pin Id	Pin #		Pin #	Pin Id
VDD	1		54	**VSS**
DQ0	2		53	**DQ7**
VDDQ	3		52	**VSSQ**
NC	4		51	**NC**
DQ1	5		50	**DQ6**
VSSQ	6		49	**VDDQ**
#CS3	7		48	**NC**
DQ2	8		47	**DQ5**
VDDQ	9		46	**VSSQ**
#CS2	10		45	**NC**
DQ3	11		44	**DQ4**
VSSQ	12		43	**VDDQ**
#CS1	13		42	**NC**
VDD	14		41	**VSS**
NC	15		40	**NC**
#WE	16		39	**DQM**
#CAS	17		38	**CLK**
#RAS	18		37	**CKE**
#CS0	19		36	**A12**
BA0	20		35	**A11**
BA1	21		34	**A9**
A10	22		33	**A8**
A0	23		32	**A7**
A1	24		31	**A6**
A2	25		30	**A5**
A3	26		29	**A4**
VDD	27		28	**VSS**

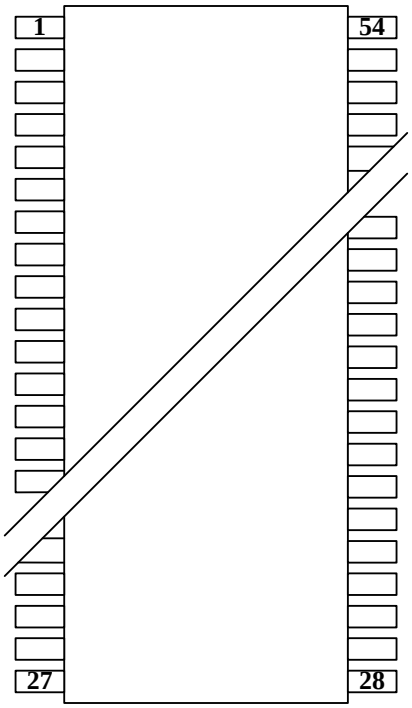

Figure 1 Pin configuration

Table 1 Pin description

Name	Function
A0~A12	Address Input. Row address (AX0 to AX12) is determined by A0 to A12 at the bank active command cycle CLK rising edge. Column address is determined by A0 to A9, A11 or A12 at the read or write command cycle CLK rising edge. And this column address becomes burst access start address.
DQ0-DQ7	Data Input/Output Ports. 8 bi-directional ports are used to read data from, or write data into the SDRAM.
#CS0 (Die1)	Die Enable Input. When #CSn is Low, the command input cycle becomes valid. When #CSn is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
#CS1 (Die2)	
#CS2 (Die3)	
#CS3 (Die4)	
BA0,BA1	BA0 and BA1 are bank select signal (BS).
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.

Name	Function
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
WE	Write Enable Input.. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
DQM	DQM controls input/output buffers. Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. (The latency of DQM during reading is 2 clocks.) Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written. (The latency of DQM during writing is 0 clock.)
CLK	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE0~CKE3	Clock enable. This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self-refresh mode.
V_{DD}	Power supply, connect to 3.3V. V_{DD} are power supply pins for internal circuits.
V_{DDQ}	Power supply, connect to 3.3V. V_{DDQ} are power supply pins for the output circuits.
V_{SS}	Ground. V_{SS} are power supply pins for internal circuits
V_{SSQ}	Ground. V_{SSQ} are power supply pins for the output circuits.
NC	No connect
Note: A10 defines the precharge mode. When A10=High at the precharge command cycle, all banks are precharged. But when A10=Low at the precharge command cycle, only the bank that is selected by BA0 and BA1 (BS) is precharged. For details refer to the command operation section.	

5 ELECTRICIAL SPECIFICATIONS

- All voltages are referenced to V_{SS} (GND).
- After power up, execute power up sequence and initialization sequence before proper device operation is achieved (refer to the Power-up Sequence).

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-0.5 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ V_{DD} +0.5 (≤ 4.6（max）)	V
Power Dissipation	P_D	2.0	W
Operating Temperature Range	T_{OPR}	-55 ~ +105	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage/ DQ power	V_{DD}/ V_{DDQ}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.8	V

5.3 DC Characteristics

Table 4 DC characteristic

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	VDD=3.0V, I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	VDD=3.6V, I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION

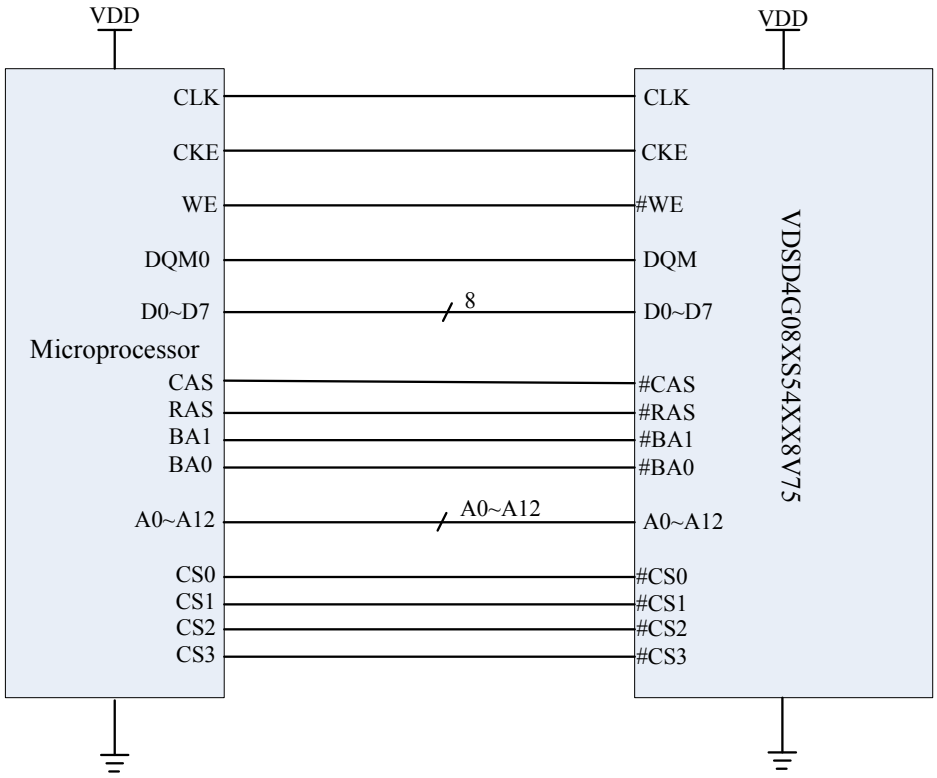

Figure 2 Typical Application

7 ORDERING INFORMATION

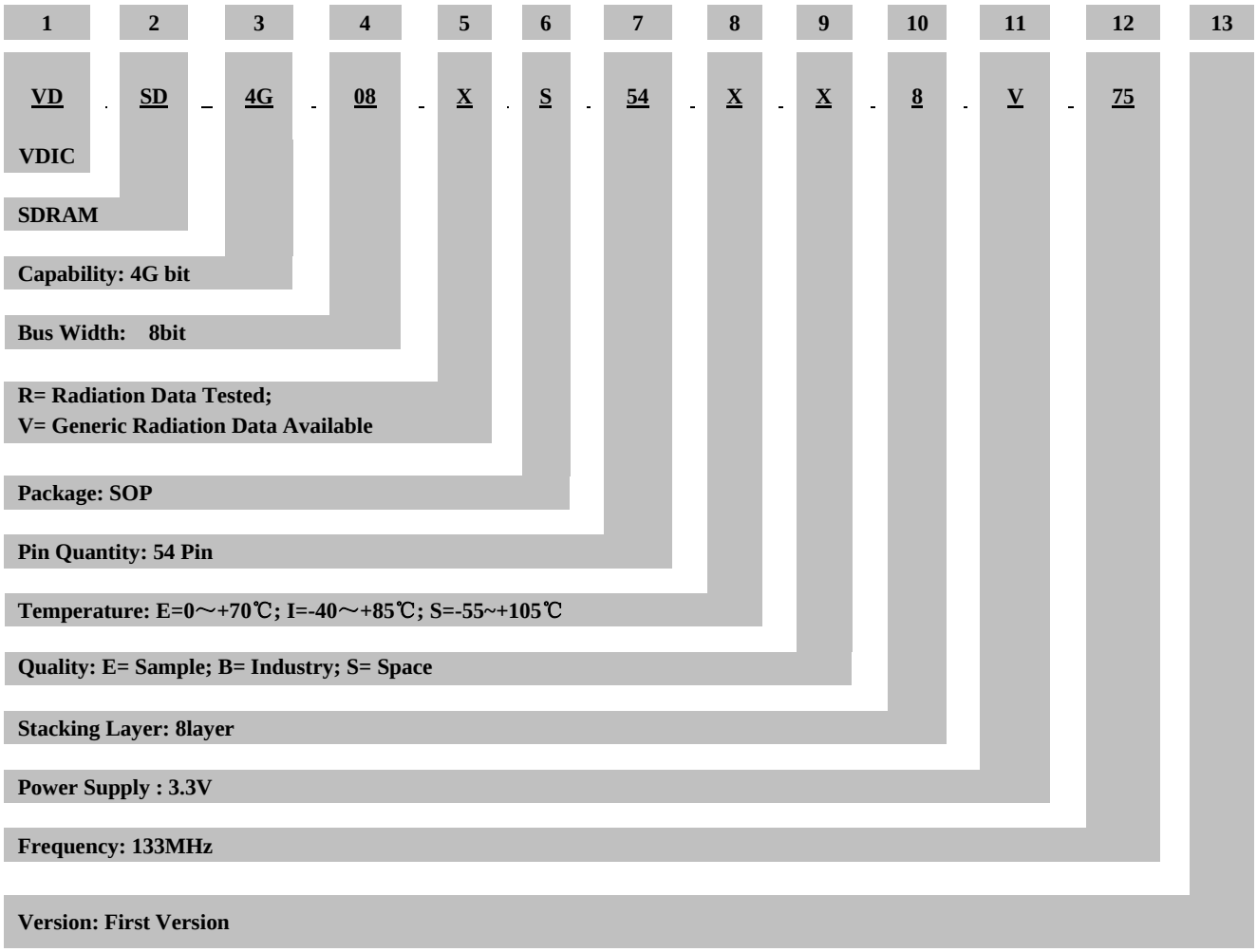

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD4G08VS54EE8V75	4G	8	-	-	-	SOP54	0 ~ + 70
VDSD4G08VS54IB8V75	4G	8	-	-	-	SOP54	-40 ~ + 85
VDSD4G08RS54SS8V75	4G	8	>50	TBD	TBD	SOP54	-55 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS

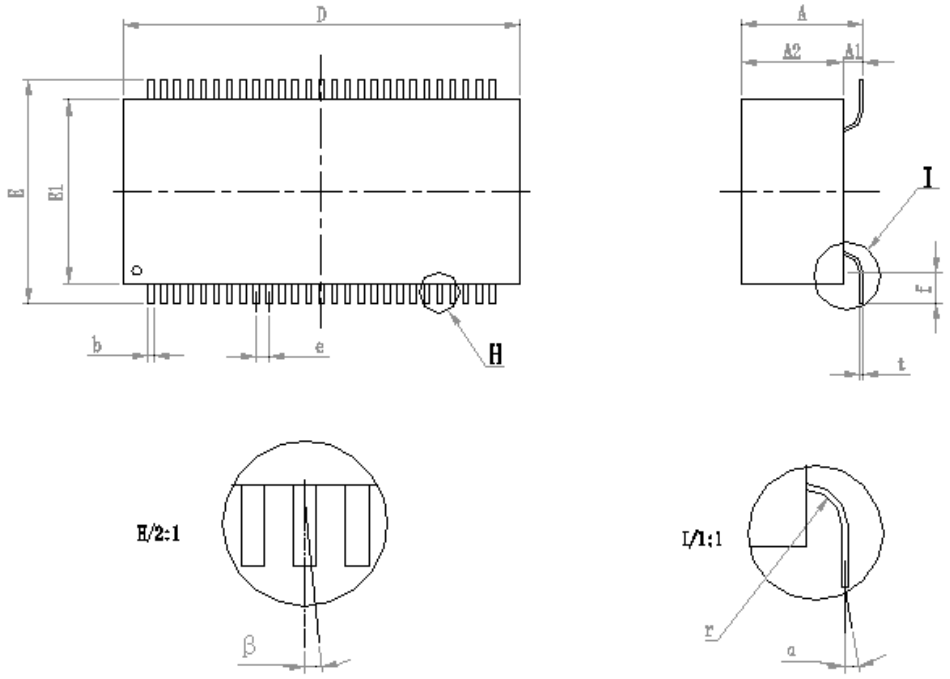

Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9 REVISION HISTORY

Table 7 Revision History

Revision	Date	Description
A0	Nov 3,2015	Initial Release
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the Truth Table
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Apr 11,2018	Modified ORDERING INFORMATION
B0	Mar 19,2020	Update TID and SEE