

VDIC ASYNCHRONOUS STATIC RAM

VDSR8M32XS64XX2V12 USER MANUAL

Version : B0

Document NO.: ORBITA/SIP-VDSR8M32XS64XX2V12-USM-01

Zhuhai Orbita Aerospace Science & Technology Co. , Ltd.

Add: Orbita Tech Park, NO.1 Baisha Road, Tangjia Dong ` an,

Zhuhai, Guangdong, China 519080

Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

1	Description.....	1
2	Features.....	1
3	Block Diagram.....	2
4	Pin Descriptions.....	2
5	Command Operation.....	3
5.1	Absolute Maximum Ratings.....	3
5.2	Recommended DC Operating Conditions.....	3
5.3	DC Characteristics.....	4
6	Typical Application.....	4
7	Ordering Information.....	5
8	Package Dimensions.....	6
9	REVISION HISTORY.....	7

VDIC-SRAM

HIGH-SPEED 256K× 32bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR8M32XS64XX2V12 is a high-speed highly integrated Static Random Access Memory containing 8.388.608bits.It is organized with two banks of 4Mbit.Each bank has 16-bit interface and is selected with specific #CS.It is particularly well suites for use in high reliability,high performance and high density system applications,such an solid state mass recorder,server or workstation.

The VDSR8M32XS64XX2V12 is available in 64-pin SOP package.

2 Features

- Single 3.3V±0.3V power supply
- Fast Access time: 12ns
- Power Dissipation :
Standy 30 mA
Operating 260mA(Max)
- TTL Compatible Input and Outputs
- Fully Static Operation
No clock or Refresh required
- Three State Outputs
- Center Power / Ground Pin Configuration.
- Die control : #CS0, #CS1,chip select

3 Block Diagram

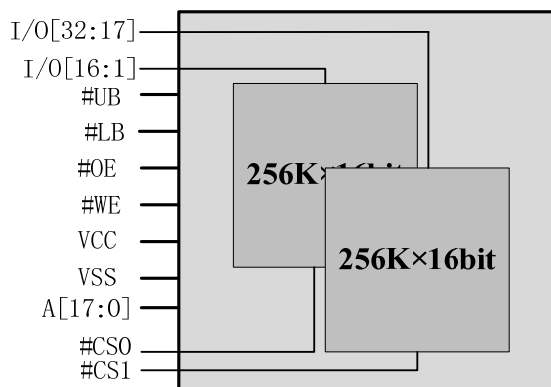


Figure 1 Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
I/O19	1	64	NC
I/O18	2	63	I/O29
I/O17	3	62	I/O30
#CS1	4	61	I/O31
NC	5	60	I/O32
A0	6	59	A17
A1	7	58	A16
A2	8	57	A15
A3	9	56	#OE
A4	10	55	#UB
#CS0	11	54	#LB
I/O1	12	53	I/O16
I/O2	13	52	I/O15
I/O3	14	51	I/O14
I/O4	15	50	I/O13
VCC	16	49	VSS
VSS	17	48	VCC
I/O5	18	47	I/O12
I/O6	19	46	I/O11
I/O7	20	45	I/O10
I/O8	21	44	I/O9
#WE	22	43	NC
A5	23	42	A14
A6	24	41	A13
A7	25	40	A12
A8	26	39	A11
A9	27	38	A10
I/O24	28	37	I/O25
I/O23	29	36	I/O26
I/O22	30	35	I/O27
I/O21	31	34	I/O28
I/O20	32	33	NC

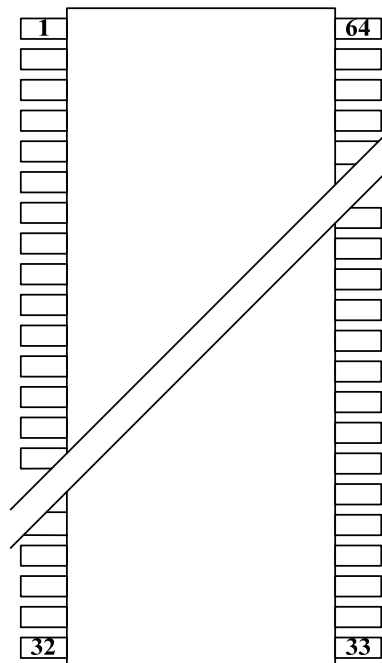


Figure 1 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0	Chip select	Disables or enables memory chip1 operation
#CS1	Chip select	Disables or enables memory chip2 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all chips
#OE	Output enable	Enables data output command to all chips
#UB	Upper byte select	Latches upper bytes data(I/O[16:9],I/O[32:25]) to all chips
#LB	Lower byte select	Latches lower bytes data (I/O[8:1],I/O[24:17]) to all chips
I/O1 ~ I/O32	Data input/output	Data inputs/outputs 32-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	V
Voltage on any pin relative to V _{SS}	V _{IN}	-0.5 to +V _{CC} +0.5	V
Power Dissipation	P _D	1.0	W
Operating Temperature Range	T _{OPR}	-55 to +125	°C
Storage Temperature Range	T _{STG}	-65 to +150	°C

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.0	—	V _{CC} +0.5	V
Input low voltage	V _{IL}	-0.5	—	0.8	V

5.3 DC Characteristics

Table 4 DC characteristics

PARAMETERS	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V _{OL}	V _{CC} =3.6V, I _{OL} =1mA	—	0.4	V
Output voltage high level	V _{OH}	V _{CC} =3.0V, I _{OH} =-0.5mA	2.4	—	V

6 Typical Application

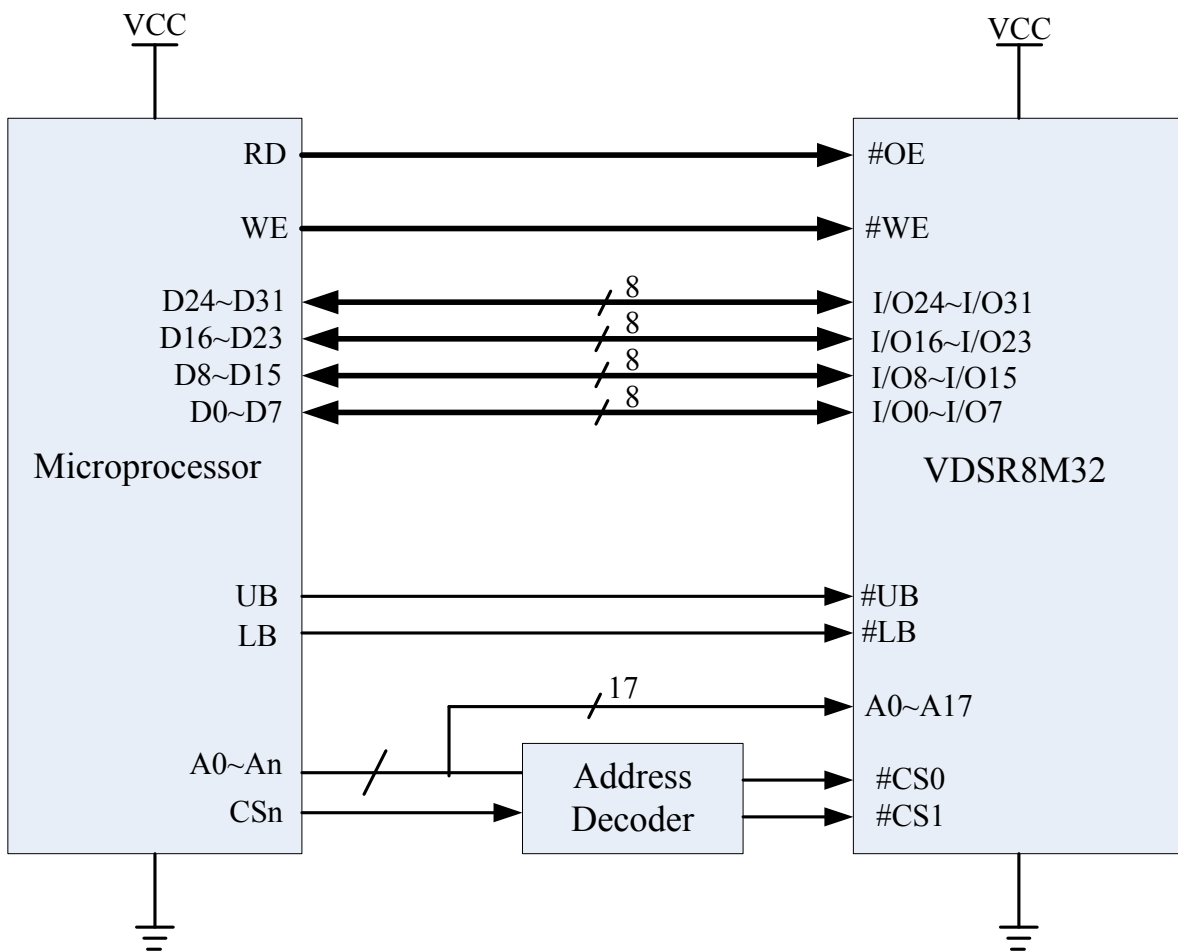


Figure 2 Typical application

7 Ordering Information

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>SR</u>	<u>8M</u>	<u>32</u>	<u>X</u>	<u>S</u>	<u>64</u>	<u>X</u>	<u>X</u>	<u>2</u>	<u>V</u>	<u>12</u>	-
VDIC												
SRAM												
Capability: 8M bit												
Bus Width: 32bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 64 Pin												
Temperature: E=0~+70°C; I=-40~+85°C; M=-55~+125°C												
Quality: E= Sample; B= Industry; M=Military; S= Space												
Stacking Layer: 2layer												
Power Supply : 3.3V												
Speed: 12ns												
Version: First Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSR8M32VS64EE2V12	8M	32	-	-	-	SOP64	0 ~ + 70
VDSR8M32VS64IB2V12	8M	32	-	-	-	SOP64	-40 ~ + 85
VDSR8M32VS64MM2V12	8M	32	-	-	-	SOP64	-55 ~ + 125
VDSR8M32RS64MS2V12	8M	32	> 100	> 75	> 0.9	SOP64	-55 ~ + 125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm2/mg)

³ SEU:SEU Threshold (Mev.cm2/mg)

8 Package Dimensions

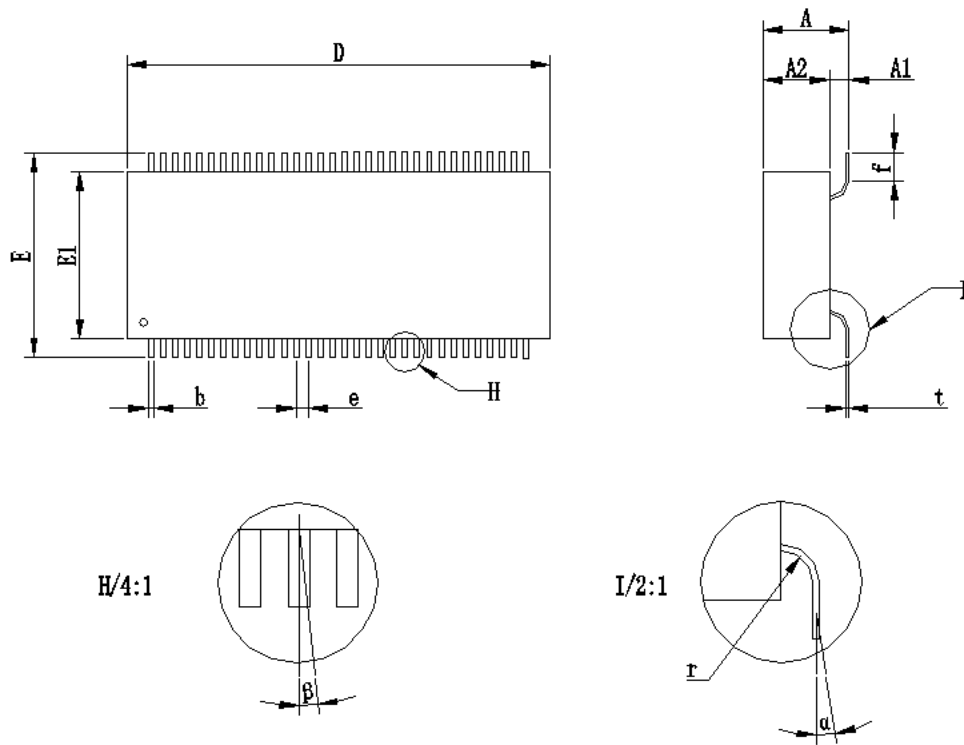


Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	5.20	5.70
A2	4.00	4.40
D	27.80	28.20
E	13.40	13.80
E1	10.80	11.20
f	2.0	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1=A-A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Apr 13,2018	Add or reduce chapters
A2	Oct 18,2018	Revising pin descriptions and block diagram
B0	Mar 21,2020	Update TID and SEE